SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

Simple Reset Circuits for the ST62

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INTRODUCTION

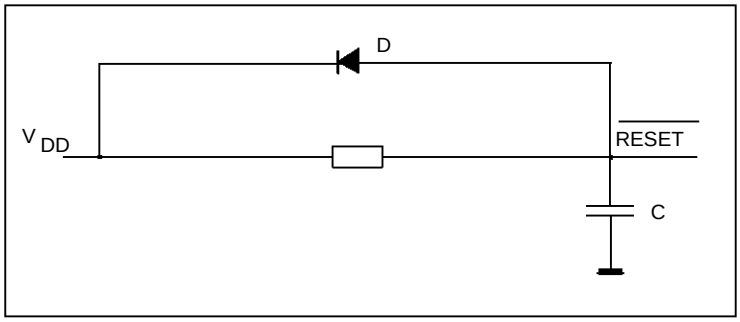
The following circuit schematics show examples of reset circuits for the ST62xx microcontrollers. These circuits range from a very simple solution, which is only efficient at power down, to a circuit providing power up and power down monitoring with a delay at power on. When used with the watchdog Timer and a software implementation, an efficient and reliable reset of the ST62 can be made.

The second part of this note presents a program which takes advantage of the presence of a watchdog inside the ST62 microcontroller to prevent a loss of functions in case of bad or noisy reset input signal.

1 HARDWARE IMPLEMENTATIONS

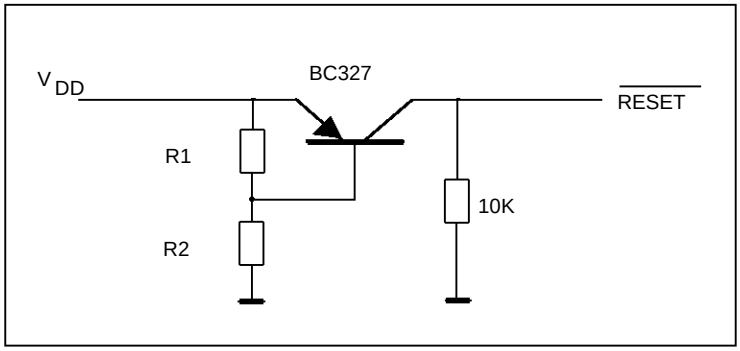
The RESET signal should not go high if the voltage supply is outside the microcontroller frequency/voltage range

a)



- Simple and cost effective, but is active only at power on.
- Needs a delay between two successive power-on cycles to discharge C.

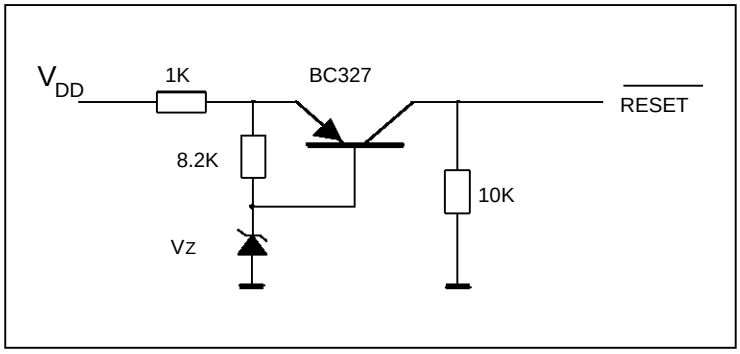
b)



- Reset signal is held low at both Power on and Power off for security.
- Monitored voltage:

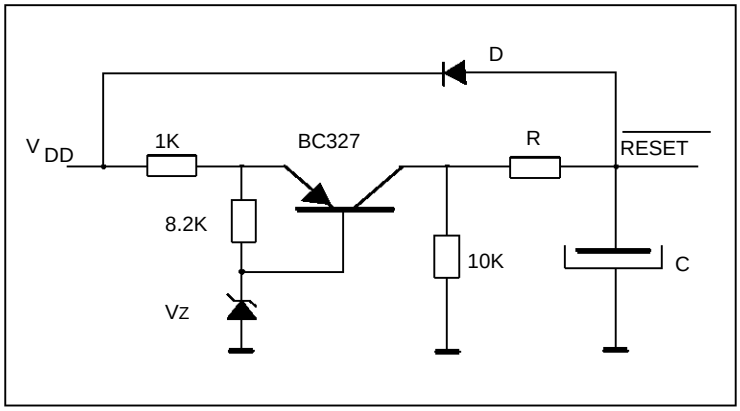
$$VS + 0.6 \times \frac{R1 + R2}{R1}$$

c)



- Similar to b), but with slightly more precise voltage switching.
- Monitored voltage:
  $V_S = V_Z$

d)



- Reset signal is held active at both Power on and Power off.
- Delay at Power on and Power off determined by the time constant of RC.
- Monitored voltage:
  $V_S = V_Z$

With the internal configuration of the ST62 I/O pins, the diode d can be externally suppressed.

Software implementation

To prevent a loss of function from a bad or noisy reset input, a software loop lasting approximately 20ms can be implemented immediately after the reset. In this loop, within the first few instructions, the Watchdog Timer is activated with a short time-out delay.

If, during this loop, the ST62 program gets lost due to an incorrect reset, the Watchdog will time-out and provide a further clean reset. This will continue until the program exits the delay with correct operation.

EXAMPLE RESET ROUTINE

```
<Software>

      start
            ldi   wdt,10000011b    ; start watchdog for 384uS
            ldi   count,0
      n1
            ldi   wdt,10000011b
            ldi   a,0

      n2    inc   a                ; 19 x 16.25uS = 338uS
            cpi   a,19
            jrc   n2

      inc   count
      ld    a,count
      cpi   a,59                   ; 59 x 338us = 19.9mS
      jrc   n1

; program starts here
; CAUTION, watchdog is now activated forever

      ldi   wdt,11111111b
      ...
      ...
      ...
      ldi   wdt,11111111b
      ...
      ...
      ...
      ldi   wdt,11111111b
      ...
      ...
      ...
```

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